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Possibility of Freely Achievable Multilevel Storage of Phase-Change Memory by Staircase-Shaped Pulse Programming

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We investigate the effect of the staircase-shaped pulse with two subpulses on programming characteristics in the double-layered phase-change memory for freely achievable multilevel storage. Phase-change material is melted during the first subpulse and the second one is used for controlling the total crystallinity after melting because it generally acts as crystallization time. Our finite-element analysis shows that the shorter the second subpulse is, the lower the crystallinity is. It is experimentally demonstrated that the device resistance increases with decreasing the width of the second subpulse owing to the decreasing crystallinity. This implies that any resistance levels are expected to be freely achieved by staircase-shaped pulse programming. © 2011 The Japan Society of Applied Physics

1. Introduction

Next-generation memory is expected to be characterized by fast speed, high density, nonvolatility and low power consumption. It is believed that the current mainstream flash memory has many disadvantages such as long programming time and limited cycle endurance.[1)] In particular, scaling down the flash memory to nanometer cell sizes is a critical technical problem owing to pressing reliability concerns and geometrical limitations. To solve these technical problems, some prospective memories, such as nanocrystal memory,[2)] ferroelectric memory (FeRAM),[3)] magnetoresistive memory (MRAM),[4)] phase-change memory (PRAM, or PCM),[5–7)] resistive memory (RRAM),[8,9)] and atomic switch[10)] have been proposed and widely researched.

In these promising technologies, PCM has attracted much attention all over the world because of its excellent performance.[1,6,7)] PCM is based on fast and reversible amorphous-crystalline phase transition, which leads to a significant resistance difference of around 4–6 orders of magnitude.[11–13)] It is also widely regarded as the most possible candidate for the replacement of flash memory, and significant advances have been made in exploring the limits of PCM in recent years. Bruns *et al.* reported that crystallizing the phase-change material of GeTe can increase the speed to even as fast as 1 ns and thus ultrafast memory can be expected in the future.[14)] Raoux *et al.* also demonstrated that phase-change can reliably occur at phase-change material cross sections with extremely small dimensions of as low as $3 \times 20\,\mathrm{nm}^2$, indicating the excellent scalability of the memory cell.[15)] It was discovered by our group that 16 distinguishable resistance levels can be readily created by controlling the total crystallinity in a PCM device, allowing greatly increased density in the future.[16,17)]

Although ultramutilevel storage was easily realized in our proposed double-layered memory cell, the transition among these levels is yet a technical problem for application. The multilevel storage was demonstrated by applying increasing currents for gradual crystallization from the as-deposited amorphous state. This programming method showed great difficulty in switching back to the programmed resistance level from a low-resistance crystallized level by simply applying currents. In this work, we report the effect of the staircase-shaped pulse with two subpulses on programming characteristics in the double-layered PCM for freely achievable multilevel storage.

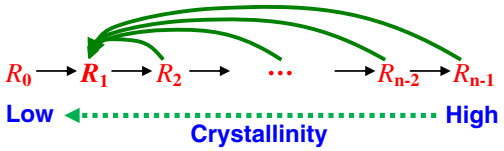

Fig. 1. (Color online) State transition of freely achievable multilevel storage by controlling the total crystallinity of the phase-change layer in a PCM device. For example, the resistance level R_1 can be freely achieved from any other resistance level.

2. Concept of Freely Achievable Multilevel Storage

The concept of freely achievable multilevel storage can be schematically illustrated as shown in Fig. 1. A high resistance level with a low crystallinity can be switched to a low resistance level by increasing the total crystallinity in the device. These easy transitions via our previous current-sweep programming are shown as black arrows between any two neighboring resistance levels, starting with the high-resistance amorphous state R_0. However, for a practical memory, it is certainly expected that any resistance level can be reached freely from any other level. For example, the resistance level R_1 can be reached only from the higher resistance level R_0 with our previous current-sweep programming. To realize a fast overwrite multilevel storage memory, however, R_1 must be reached not only from the higher resistance level (R_0) with a lower crystallinity but also from any other lower resistance levels ($R_2, \ldots, R_{n-1}$) with higher crystallinities.

The detailed approach to freely achievable multilevel storage can be further explained with programming methods in Fig. 2. As is well known, a high and short electrical pulse, as shown in Fig. 2(a), heats the phase-change material above the melting point (T_m) and then cools it suddenly, as shown in Fig. 2(d), resulting in a completely amorphous phase with the lowest crystallinity, as shown in Fig. 2(g). On the other hand, an intermediate and long electrical pulse, as shown in Fig. 2(b), heats the phase-change material between the melting point and the crystallization temperature (T_c) and maintains that temperature for a certain period, as shown in Fig. 2(e), leading to the completely crystalline phase with the highest crystallinity, as shown in Fig. 2(h). Here, we

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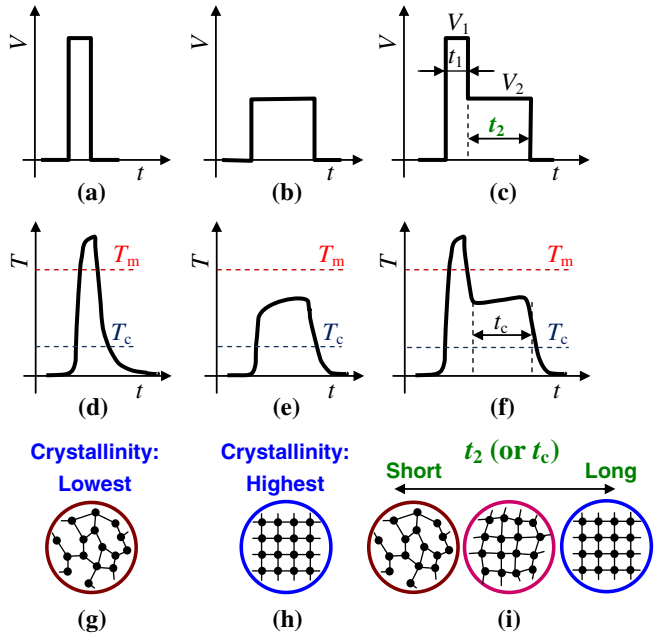

Fig. 2. (Color online) Concept of control of total crystallinity for freely achievable multilevel storage. (a) High and short pulses. (b) Intermediate and long pulse. (c) Staircase-shaped pulse. The high and short first subpulse with a time of t_1 and an amplitude of V_1 is used for amorphization of phase-change material. The intermediate and long second subpulse with a time of t_2 and an amplitude of V_2 is then used for the control of total crystallinity after melting. (d), (e), and (f) Corresponding schematic temperature profiles of (a), (b), and (c), respectively. (g), (h), and (i) Corresponding schematic atomic arrangements of (d), (e), and (f), respectively.

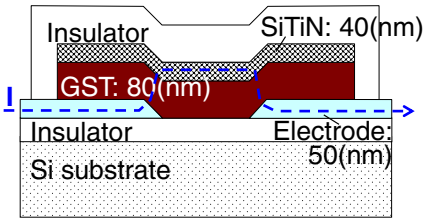

Fig. 3. (Color online) Schematic diagram of the lateral double-layered device structure.

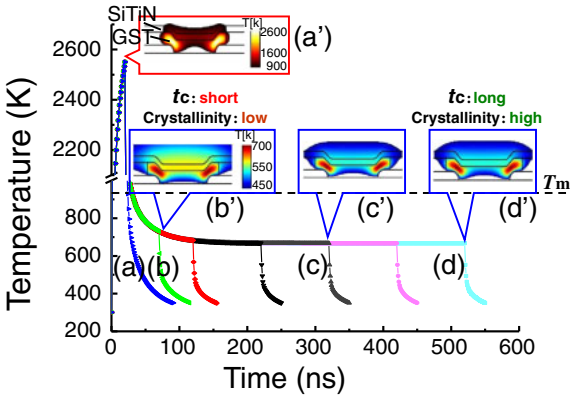

Fig. 4. (Color online) Simulation results of temperature profiles induced by staircase-shaped pulses with different second subpulse widths of 0–500 ns in the lateral double-layered device structure. (a–d) Temperature profiles for pulses with second subpulse widths of 0, 50, 300, and 500 ns, respectively. (a′–d′) Temperature distributions when the temperature starts to fall for pulses with different second subpulse widths of 0, 50, 300, and 500 ns, respectively.

proposed a staircase-shaped pulse, as shown in Fig. 2(c), to first heat the phase-change material above T_m and then allow it to cool and maintain a temperature between T_m and T_c for a certain annealing period of t_c, as shown in Fig. 2(f). The staircase-shaped pulse is composed of two subpulses for amorphization and subsequent control in crystallinity. The first amorphization subpulse with an amplitude of V_1 and a pulse width of t_1 is used for amorphizing the phase-change material, and the second crystallinity-control subpulse with an amplitude of V_2 and pulse width of t_2 is used for controlling the total crystallinity from completely amorphous to completely crystalline phases, as shown in Fig. 2(i). The two parameters of V_2 and t_2 of the second subpulse are of great importance for the control of the total crystallinity via the annealing temperature and time (t_c). Here, we mainly discuss the effect of the width t_2 of the second subpulse on the total crystallinity for freely achievable multilevel storage.

3. Results and Discussion

A lateral double-layered device structure,[16,18] as shown in Fig. 3, was adopted in this work. The thicknesses of SiTiN, $Ge_2Sb_2Te_5$ (GST), and TiN electrodes are 40, 80, and 50 nm, respectively. The gap length between electrodes is 400–3000 nm. The GST, and SiTiN layers were deposited using radio-frequency sputtering equipment (ULVAC MNS-3000-RF) at a background pressure below 5×10^{-5} Pa and a sputtering pressure of 0.2 Pa. For the SiTiN film, the gas flow rates of N_2 and Ar simultaneously introduced into the chamber during sputtering were 1 and 14 sccm, respectively. A waveform generator (Tabor Electronics 2571) was adopted to apply single staircase-shaped pulses to the devices. Device resistance R was read out at a low voltage.

Figure 4 shows the highest temperature profile simulated using commercially available finite-element analysis software COMSOL 3.3. Curve (a) shows the temperature profile induced by the simplest pulse ($t_2 = 0$) of 11 V, 20 ns. The temperature distribution is shown in the inset of Fig. 4(a′). The region between electrodes is heated above the melting point (around 905 K for the GST film[19–21]). The quench time from the melting point to the crystallization temperature (around 433 K for the GST film[22–24]) is 20–30 ns, which is long enough to amorphize the phase-change material.[1)] Then the annealing time can be controlled by applying a staircase-shaped pulse with 11 V, 20 ns for the first subpulse and 4 V for the second subpulse with a time of 50–500 ns. Simulated results exhibit similar temperature distributions for these stair-like shaped pulses. Typical temperature distributions for pulses with second subpulse times of 50, 300, and 500 ns are shown in Figs. 4(b′), 4(c′), and 4(d′), respectively. This means that the annealing time can be controlled simply by the time of the second subpulse. As is well known for the phase-change films, the shorter the annealing time t_c at a certain temperature, the lower the crystallinity.[25] A low crystallinity corresponds to a high device resistance in a PCM device.

The experimental results of relative resistance change R/R_{asdepo} after switchings are shown in Fig. 5. The

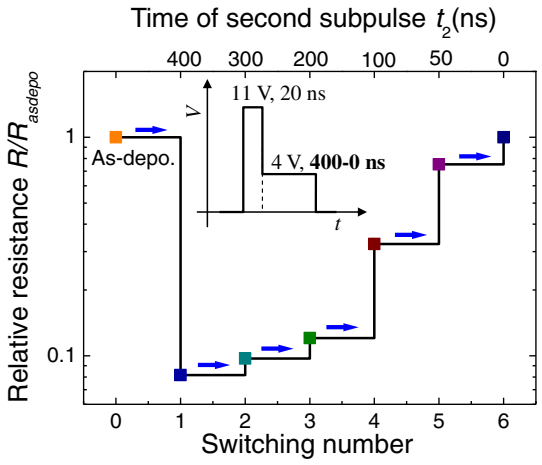

Fig. 5. (Color online) Experimental results of transitions of resistance level induced by staircase-shaped pulses with different second subpulse widths of 0–400 ns in a lateral device structure. Total crystallinity for freely achievable multilevel storage can be controlled by adjusting the time of second subpulse.

resistance started with the as-deposited state, corresponding to R_0. After applying a crystallization pulse, the device was first crystallized from the as-deposited state and R/R_{asdepo} correspondingly dropped to 0.082. Then staircase-shaped pulses with the first subpulse of 11 V, 20 ns and a second subpulse of 4 V, 400–0 ns were applied to the device. After applying a pulse with a 300 ns second subpulse, the device resistance increased from 46 to 55 kΩ and R/R_{asdepo} correspondingly increased from 0.082 to 0.097. The device resistance further increased to 68 kΩ after applying a pulse with a shorter 200 ns second subpulse. R/R_{asdepo} correspondingly increased to 0.121. The application of a pulse with a 100 ns second subpulse results in a resistance increase to 185 kΩ. R/R_{asdepo} correspondingly increased to 0.325. The pulse with a 0 ns second subpulse finally made the resistance change from 427 to 568 kΩ. R/R_{asdepo} correspondingly increased from 0.752 to 1. As we can see, the resistance level with a low cystallinity can be reversibly switched back from a resistance level with a higher cystallinity by applying a staircase-shaped pulse with a suitable second subpulse width.

It is believed that the programming with staircase-shaped pulses opens the way to freely achievable multilevel storage. Varied pulses with different pulse amplitudes of the second subpulses can also be expected to control the crystallinity for freely achievable multilevel storage; this is still under investigation. In the future, we expect that fast freely achievable multilevel storage can be realized by applying staircase-shaped pulses with both suitable pulse amplitudes and suitable pulse widths of the second subpulses.

4. Conclusion

The staircase-shaped pulse with two subpulses was proposed for programming the double-layered phase-change memory for freely achievable multilevel storage. The second subpulse is critical in controlling the total crystallinity, according to our simulation results. Experimental results show that the device resistance increases on reducing the width of the second subpulse owing to the decreasing crystallinity. This staircase-shaped pulse programming technique exhibited the possibility that any resistance level can be freely achieved.

Acknowledgments

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